REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Final Action and respectfully requests reconsideration of this application in view of the foregoing amendments and the following remarks. The Applicant originally submitted Claims 1-20 in the application. The Applicant amended Claims 1, 8 and 15 in response to a previous examiner's action, but has not amended any claims in response to the present Examiner's Action. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejection of Claims 1-20 under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,651,125 to Witt, *et al.*, in view of U.S. Patent 3,863,225 to Preiss. With respect to Claims 1 and 8, the Examiner asserts that Witt teaches categorization logic, associated with an earlier pipeline stage and priority logic, associated with a later pipeline stage, but does not teach the element of allocating functional units in a processor based on a predefined priority of functional units. The Examiner cites Preiss for this missing element and asserts that the combination of Witt and Preiss would be obvious to one skilled in the art.

The Applicant traverses the Examiner's rejection of Claims 1 and 8. While both Witt and Preiss apply generally to processor architecture, it would not be obvious to one skilled in the art to combine Witt's categorization and priority logic with Preiss's predefined functional unit priority. Witt teaches a general-purpose microprocessor architecture, specifically a RISC architecture. Column 10, lines 36-41. Such a processor is designed for the general requirements of a modern microcomputer system, such as computation, I/O and memory management. This architecture is based on a common data bus (CDB) with multiple functional units (FUs), with allocation of

functional units accomplished by means of reservation stations. All these basic elements are well known to those skilled in the art of microprocessor design. Witt focuses on a narrow improvement of increased speed and space efficiency by sharing key components and coupling the integer unit and floating point unit to the CDB.

Allocation of the functional units based on a predefined priority of the functional units would not achieve Witt's inventive objective. First, such a scheme would not result in increased efficiency of the disclosed general-purpose architecture. Each FU has a dedicated instruction queue (reservation station) to allow the instruction issue logic to view the processor as having a larger number of virtual functional units. Instructions are issued to the appropriate FU as long as the reservation station is not full. Adding a predefined priority to the functional units is not compatible with Witt's architecture. While such an addition might not cause the architecture to fail, it would add no value to the architecture in its disclosed form. Moreover, the logic required to implement the predefined priority would consume incremental power and "real estate" on the microprocessor die, so would be disadvantageous without a compelling reason to include it. Thus one skilled in the art would not be motivated to add a predefined priority to the functional units to Witt's architecture. Thus, the combination of Witt and Preiss is improper.

Moreover, Preiss is concerned with an unrelated area of processor design. Preiss seeks to increase the efficiency of then-known priority control schemes. As described above, priority control does not have utility in an architecture based on reservation stations and a common data bus. Thus, one seeking to increase the speed of operation of a RISC processor would have no motivation whatsoever to look to Preiss. For this reason also, the combination of Witt and Preiss is not proper and the rejection of Claims 1 and 8 is improper.

The Examiner also asserts that Witt anticipates Claim 4, 11 and 18, which claim the element of ungrouping of instructions when the categorization logic generates instruction type information. However, Witt is utterly silent regarding grouping and ungrouping of instructions. Furthermore, Witt contains no suggestion either to group or ungroup instructions. Table II of Witt lists pipeline stages applicable to a superscaler microprocessor, but it only includes fetch, decode, execute, result forward and writeback stages. The Examiner does not cite Preiss in rejecting these claims, so the combination of Witt and Preiss does not teach or suggest ungrouping of instructions. Claims 4, 11 and 18 are allowable.

The Examiner asserts that Witt anticipates Claim 6, 13 and 20, which claim the element of the priority logic employing separate allocation schemes depending upon categories defined by the instruction type information associated with an instruction. The present application discloses an embodiment that employs two such schemes in FIGUREs 5 and 6. The scheme described by FIGURE 5 is employed for the instruction located in slot 1 (element 410) of categorization queue 400, for which any functional unit may be assigned, as none are in use when a functional unit is assigned to this instruction. Specification, ¶ 0055. The scheme described by FIGURE 6 is employed for instructions of lower priority in categorization queue 400, because one or more functional units may be in use when the lower priority instruction is assigned. Id. The Examiner asserts that Witt teaches multiple allocation schemes by providing, for example, that a shift-type opcode may be allocated to the shifter FU, while a branch-type opcode may be allocated to the branch FU. Unfortunately, the argument is unfounded. While Witt may teach that different type opcodes may be allocated to their corresponding functional units, this describes a single scheme, *i.e.*, a scheme in which an opcode is routed to the appropriate FU depending on its instruction tag. The present application describes two, clearly demonstrably different schemes in the form of the flow charts

shown in FIGUREs 5 and 6, whereas Witt is silent regarding a scheme in addition to the fundamental scheme of FU allocation. Nor is there any suggestion in Witt of multiple allocation schemes. Witt employs reservation stations to queue instructions at each FU, so as a general case, there will not be an occurrence for which no functional units are assigned. Furthermore, the Examiner fails to cite Preiss when rejecting these claims, so the combination of Witt and Preiss fails to teach or suggest separate allocation schemes. Claims 6, 13 and 20 are allowable.

The Examiner rejects Claims 7 and 14, asserting that Witt teaches the use of the mechanism of Claim 1 in a digital signal processor (DSP). The Applicant again disagrees. As described previously, Witt teaches and is concerned with, an architecture for a RISC processor. A RISC processor is a general-purpose processor designed to accomplish various tasks in as efficient a manner as possible, but its general-purpose nature results in greater use of space on the die, higher power consumption and other design tradeoffs. By contrast, a DSP is designed to efficiently implement an algorithm to alter a real-time data stream (video or audio, *e.g.*) on a small die with minimal power consumption. A RISC processor is not a DSP. For example, one would not put a RISC processor in a cell phone. The Examiner does not cite Preiss in rejecting these claims, so the combination of Witt and Preiss fails to teach or suggest using the present invention, as Claim 1 defines it, in a DSP. Thus, Claims 7 and 14 are allowable.

Finally, the Examiner rejects Claim 15, again asserting that Witt teaches a DSP, that Preiss teaches allocating functional units based on a predefined priority of functional units and that the combination of Witt and Preiss would be obvious to one skilled in the art. For the reasons discussed previously, Witt does not teach a DSP. Furthermore, one skilled in the art would not look to Preiss to increase the speed of operation of a RISC processor. Therefore, Claim 15 is allowable.

III. Conclusion

In view of the foregoing amendments and remarks, the Applicant now sees all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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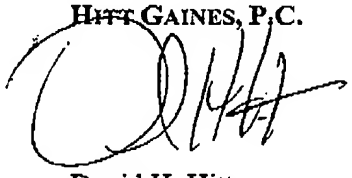

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